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10/562,800	12/29/2005	Chuichi Miyazaki	1374.45693X00	8700

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EXAMINER	
NGUYEN, DUY T V	

ART UNIT	PAPER NUMBER
2894	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,800	MIYAZAKI ET AL.	
	Examiner	Art Unit	
	DUY T. NGUYEN	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/29/08, 12/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Abstract

1. The abstract of the disclosure is objected to because the abstract may not exceed 150 in length. Correction is required. See MPEP § 608.01(b).

Specification

2. The specification is objected because of the flowing reasons:

Regarding to abstract, lines 4, 5, 8-11: please replace square boxes with “micron" or "um” according to PCT publication.

Regarding to the specification, pages 3, 5, 6, 14-18, 20-22, 29, 34 please replace square boxes with “micron" or "um” according to PCT publication.

Appropriate correction is required.

Claim Objections

3. The claims are objected because of the following reasons:

Regarding claims 6-11 and 17-22, line 3: please replace square boxes with “micron" or "um”.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoon et al. (US 2005/0079687, from hereinafter "Yoon").

Regarding claim 1, Yoon teaches, as shown in Figs. 1a-c, 2a-2d, and 4, a manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a circuit pattern [0006] over a first main surface of a semiconductor wafer (10) that has a first thickness (actual thickness before grinding step) [0008];

(b) making the semiconductor wafer a second thickness (thickness after first polished step) [0008] by grinding a second main surface of the semiconductor wafer (10) using a first grinding material [0008] which has a fixed abrasive;

(c) making the semiconductor wafer a fourth thickness (thickness after sand blasting step) ([0030] and Table 1) by grinding the second main surface of the semiconductor wafer (10) using a third grinding material [0030] which has a fixed abrasive a diameter of a particle of which is smaller than the first grinding material [0008], [0030]; and

(d) individually separating the semiconductor wafer to a chip by dicing the semiconductor wafer [0008].

Although, Yoon fails to explicitly teach a second crush layer and a particle size of a polish fine powder of the third grinding material is #3000 to #100000; Yoon does teach rough surfaces (created after grinding, polishing and sand-blasting steps) ([0008], [0024], [0025] and Table 1), and a particle size of a polish fine powder of the third grinding material [0008] and Table 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ and modify the teaching as taught by Yoon to have a crush layer formed in the second main surface of the semiconductor wafer and a particle

size of a polish fine powder of the third grinding material is #3000 to #100000, because it aids in reducing unit cost of the chip and increasing productivity [0033].

Regarding claims 2-5, Yoon fails to explicitly teach a particle size of a polish fine powder of the first grinding material is #100 to #700 (as cited in claim 2); the particle size of the polish fine powder of the third grinding material is #4000 to #50000 (as cited in claim 3); the particle size of the polish fine powder of the third grinding material is #4000 to #50000 (as cited in claim 4); and the particle size of the polish fine powder of the third grinding material is #8000 or more than it (as cited in claim 5); Yoon does teach particle sizes of first and third grinding materials [0008], [0030] and Table 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ particle size range as taught by Yoon to have a particle size of a polish fine powder of the first grinding material is #100 to #700; the particle size of the polish fine powder of the third grinding material is #4000 to #50000, the particle size of the polish fine powder of the third grinding material is #4000 to #50000; and the particle size of the polish fine powder of the third grinding material is #8000 or more than it, because particle sizes are known to affect device properties and would depend on the desired device density on the desired device characteristic. One of ordinary skill in the art would have been led to the recited particle sizes of the grinding materials through routine experiment to achieve desired characteristic of the formed IC device.

Regarding claims 6-8, referred to claim 1 for the crush layer, Yoon teaches a thickness of the second crush layer is less than 1 um (as cited in claim 6); less than 0.5 um (as cited in claim 7); and less than 0.1 um (as cited in claim 8) (see Table 1).

Regarding claims 9-11, Yoon teaches the fourth thickness of the semiconductor wafer is less than 100 um (as cited in claim 9); less than 80 um (as cited in claim 10); and less than 60 um (as cited in claim 11) ([0008], [0022], [0023] and Table 1 for reduced thickness after every 5 mins from original thickness)

Regarding claims 12 and 13, Yoon teaches (e) making the semiconductor wafer a third thickness (after second polished step) [0008] thinner than the second thickness (after first polished step) [0008] and thicker than the fourth thickness (after sand blasting step) ([0030] and Table 1) by grinding the second main surface of the semiconductor wafer using a second grinding material [0008] which has a fixed abrasive with a diameter of a particle smaller than the first grinding material [0008].

Although, Yoon fails to explicitly teach the diameter of the particle larger than the third grinding material (as cited in claim 12) and a particle size of a polish fine powder of the second grinding material is #1500 to #2000 (as cited in claim 13). Yoon does teach particle size between 3 -120 um [0008], 0023], and Table 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ and modify the teaching as taught by Yoon to have the diameter of the particle larger than the third grinding material and a particle size of a polish fine powder of the second grinding material is #1500 to #2000, because particle sizes are known to affect device properties and would depend on the desired device density on the desired device characteristic. One of ordinary skill in the art would have been led to the recited particle sizes of the grinding materials through routine experiment to achieve desired characteristic of the formed IC device.

Regarding claim 14, Yoon teaches as shown in Figs. 1a-c, 2a-2d, a manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a circuit pattern [0006] over a first main surface of a semiconductor wafer (10) that has a first thickness (actual thickness before grinding step) [0008];

(b) making the semiconductor wafer a second thickness (thickness after first polished step) [0008] by grinding a second main surface of the semiconductor wafer (10) using a first grinding material [0008] which has a fixed abrasive;

(c) making the semiconductor wafer a third thickness (thickness after second polished step) [0008] by grinding the second main surface of the semiconductor wafer (10) using a second grinding material [0008] which has a fixed abrasive a diameter of a particle of which is smaller than the first grinding material [0008]; and

(f) individually separating the semiconductor wafer to a chip by dicing the semiconductor wafer [0008].

Although, Yoon fails to explicitly teach forming a first crush layer, removing a first crush layer, and forming a third crush layer; Yoon does teach rough surfaces (created after grinding, polishing and sand-blasting steps) ([0008], [0024], [0025], [0029] and Table 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ and modify the teaching as taught by Yoon to form a first crush layer, remove a first crush layer, and form a third crush layer in the second main surface of the semiconductor wafer, because it aids in reducing unit cost of the chip and increasing productivity [0033].

Regarding claims 15 and 16, Yoon fails to explicitly teach a particle size of a polish fine powder of the first grinding material is #100 to #700 (as cited in claim 15); a particle

size of the polish fine powder of the second grinding material is #1500 to #2000 (as cited in claim 16); Yoon does teach particle sizes of first and second grinding materials [0008] and Table 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ particle size range as taught by Yoon to have a particle size of a polish fine powder of the first grinding material is #100 to #700 a particle size of the polish fine powder of the second grinding material is #1500 to #2000, because particle sizes are known to affect device properties and would depend on the desired device density on the desired device characteristic. One of ordinary skill in the art would have been led to the recited particle sizes of the grinding materials through routine experiment to achieve desired characteristic of the formed IC device.

Regarding claims 17-19, referred to claim 14 for the crush layer, Yoon teaches a thickness of the third crush layer is less than 0.5 um (as cited in claim 17); less than 0.3 um (as cited in claim 18); and less than 0.1 um (as cited in claim 19) (see Table 1).

Regarding claims 20-22, Yoon teaches the third thickness of the semiconductor wafer is less than 100 um (as cited in claim 20); less than 80 um (as cited in claim 21); and less than 60 um (as cited in claim 22) ([0008], [0022], [0023] and Table 1 for reduced thickness after every 5 mins from original thickness) .

Regarding claim 25, Yoon teaches (el) forming the third crush layer in the second main surface of the semiconductor wafer by grinding (sand blasting) the second main surface of the semiconductor wafer (Table 1 and [0029]).

Regarding claim 26, although, Yoon fails to teaches (d1) making a left-behind first crush layer the third crush layer of the step (e) by removing the first crush layer formed in

the second main surface of the semiconductor wafer leaving a part; Yoon does teach removing the first crush and making the third crush (Table 1 and ([0008], [0024], [0025], [0029]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching as taught by Yoon to make the third crush layer from a left behind first crush layer because it aids in reducing unit cost and improving productivity [0033].

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoon in view of Lee et al. (US 6,423,640, from hereinafter “Lee"). The teachings of Yoon have been discussed above.

Regarding claim 24, referred to claim 14 for the third crush layer, Yoon fails to teach forming the third crush layer in the second main surface of the semiconductor layer by injecting an abrasive particle to the second main surface of the semiconductor wafer.

Lee teaches injecting an abrasive particle to the surface of the semiconductor wafer (see abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the injecting step as taught by Lee combined with Yoon to form the third crush layer because it aids in removing metal residues and dishing/erosion defects (col. 3, lines 20-23).

6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoon in view of Savas et al. (US 2005/0059250, from hereinafter “Savas"). The teachings of Yoon have been discussed above.

Regarding claim 25, referred to claim 14 for the third crush layer, Yoon fails forming the third crush layer in the second main surface of the semiconductor wafer by impacting an ion produced by plasma electric discharge to the second main surface of the semiconductor wafer.

Savas teaches the ions from the plasma impact the wafer nearly perpendicular to the wafer surface [0006].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ and modify the teaching as taught by Savas combined with Yoon to form the third crush layer in the second main surface of the semiconductor wafer by impacting an ion produced by plasma electric discharge to the second main surface of the semiconductor wafer because it aids in providing an improved etching system and process [0016].

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DUY T. NGUYEN whose telephone number is (571) 270-7431. The examiner can normally be reached on Monday-Friday, 7:30 Am - 5:00 Pm (alternative Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on (571) 272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DUY T NGUYEN/
Examiner, Art Unit 2894

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894